

Mixed-Signal Blockset™ Release Notes



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New Features

Introducing Mixed-Signal Blockset: Design, simulate, and verify analog and mixed-signal systems

Mixed-Signal Blockset provides models of components and impairments, analysis tools, and test benches for designing and verifying mixed-signal integrated circuits (ICs).

You can model PLLs, data converters, and other systems at different levels of abstraction and explore a range of IC architectures. You can customize models to include impairments such as noise, nonlinearity, and quantization effects, and refine the system description using a top-down methodology.

Using the test benches provided, you can verify system performance and improve modeling fidelity by fitting measurement characteristics or circuit-level simulation results. Rapid system-level simulation using variable-step Mixed-Signal Blockset solvers lets you debug the implementation and identify design flaws before simulating the IC at the transistor level.

With Mixed-Signal Blockset you can simulate mixed-signal components together with complex DSP algorithms and control logic. As a result, both analog and digital design teams can work from the same executable specification.

White-Box Behavioral Models of PLL and ADC: Design and analyze mixed-signal systems based on typical architectures using data-sheet specifications

Use the provided PLL models such as Fractional N PLL with Analog Compensation, Fractional N PLL with Delta Sigma Modulator, Integer N PLL with Dual Modulus Prescaler, Integer N PLL with Single Modulus Prescaler to design and simulate your own customized PLL at the system level. Verify and visualize the open loop and closed loop responses.

Use the provided ADC architectures Flash ADC and SAR ADC to design and simulate your own customized ADC at the system level.

White-Box Building Blocks: Design custom mixed-signal systems following a top-down methodology

Mixed-Signal Blockset provides white-box building blocks that you can use to design custom mixed-signal systems. See the PLL “Building Blocks” and ADC “Building Blocks” for more information.

Models of Impairments: Model timing effects, phase noise, jitter, leakage, and other impairments

Model rise/fall times, finite slew rate, and variable time delays in your feedback loop for both PLL and ADC systems.

Model the phase noise in PLL system. For more information, see .

Model the aperture jitter, offset error, and gain error in ADCs.

Measurement Blocks and Testbenches: Verify the performance of PLL and ADC with application-specific metrics

Use the provided “Measurements and Testbenches” to

- Measure the lock time, phase noise profile, operating frequency of a PLL.
- Characterize the performance of building blocks such as VCO, PFD, and charge pump.
- Measure AC and DC characteristics and aperture jitter of ADCs.

